UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/625,751	07/23/2003	William Kenneth Waller	0302	8135

7590 03/23/2005

William K. Waller
2262 N. Greenview Ct
Eagle, ID 83616

EXAMINER	
LAM, DAVID	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 03/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/625,751	WALLER, WILLIAM KENNETH	
	Examiner	Art Unit	
	David Lam	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities:

Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of ***50 to 150 words***. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 4-5, 8-9, 11-12, 14-15 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claims 4-5, 8-9, 11-12, 14-15, the use of term "can" or "can be" renders the claims indefinite. Claims language should be written in a positive manner. It appears the "can be located" should be changing to -- located --.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maki (6,501, 694).

Regarding to claims 1- 3, Maki discloses a memory device having a complementary-logic bit line pair having true and inverted bit lines (B1, *B1); equilibrating means (P2) connected to the bit line pair, biasing means (P3), connected to only one of the bit lines; wherein when the equilibrating and biasing means are activated together, the bit line pair is thus equilibrated and biased; wherein the equilibrating means comprises a first transistor (P2) connected to the bit line pair such that when activated, the bit lines are shorted together; the biasing means comprises a second transistor (P3) connected to only one of the bit lines and connected to a biasing node, such that when activated, the one of the bit line is short to the biasing node; such that when the first and second transistors are activated together, the bit line pair is equilibrated and biased, and wherein the biasing node is located next to the second transistor. *See. Figs. 1-3; Cols. 3-5.*

Regarding to claim 6, Maki discloses a memory device having a biasing node, and first and second complementary-logic bit line pairs each having true and inverted bit lines (B1-B4, *B1- *B4); first equilibrating means (P2) able to short the bit lines of the first pair (B1, *B1) together; second equilibrating means able to short the second bit line pair (B2, *B2) together;

first biasing means (P3), able to short only one of the bit lines of the first bit line pair to the biasing node; second biasing, able to short only one of the bit lines of the second bit line pair (B2, *B2) to the biasing node; wherein the biasing node is interstitially located between the first and second biasing means. *See. Figs. 1-3; Cols. 3-5.*

As of claim 7, Maki further discloses wherein the first equilibrating means comprises first transistor (P2), connected to the first bit line pair (B1, *B1), such that the first transistor is activated, the first bit line pair is short together; the second equilibrating means comprises second transistor, connected to the second t bit line pair (B2, *B2), such that the second transistor is activated, the second bit line pair is short together; the first biasing means comprises a third transistor (P3), connected to only one of the bit lines in the first bit line pair and connected to a biasing node; such that when the third transistor is activated, the one of the bit lines of the first bit line pair is shorted to the biasing node; the second biasing means comprises a fourth transistor, connected to only one of the bit lines in the second bit line pair (B2, *B2) and connected to a biasing node; such that when the fourth transistor is activated, the one of the bit lines of the second bit line pair is shorted to the biasing node; wherein the first, second , third and fourth are activated together, thus equilibrating and biasing the bit line pairs. *See. Figs. 1-3; Cols. 3-5.*

Regarding to claim 10, Maki discloses a memory device, having: an equilibrate node; a biasing node; a complementary-logic bit line pair having true and inverted bit lines; a first transistor, connected to the bit line pair and gated by the equilibrate node such that when the equilibrate node is activated, the bit line pair is shorted together and thus equilibrated; a second transistor, connected to the true bit line and to the biasing node, and gated by the equilibrate

node, such that when the equilibrate node is activated, the true bit line is shorted to the biasing node, thus biasing the true bit line; a third transistor, connected to the inverted bit line and to the biasing node, and gated by the equilibrate node, such that when the equilibrate node is activated, the inverted bit line is shorted to the biasing node, thus biasing the inverted bit line; *(see Fig 1-2 of the prior art)*; the improvement comprising: conversion of one of the second and third transistors from a three-terminal device to a two-terminal device, allowing the biasing node to be located next to remaining unconverted of the second and third transistors, without widening circuit area. *See. Figs. 1-3; Cols. 3-5.*

As of claim 13, Maki discloses a memory device, having: an equilibrate node; a biasing node; a complementary-logic bit line pair having true and inverted bit lines; a first transistor, connected to the bit line pair and gated by the equilibrate node such that when the equilibrate node is activated, the bit line pair is shorted together and thus equilibrated; a second transistor, connected to the true bit line and to the biasing node, and gated by the equilibrate node, such that when the equilibrate node is activated, the true bit line is shorted to the biasing node, thus biasing the true bit line; a third transistor, connected to the inverted bit line and to the biasing node, and gated by the equilibrate node, such that when the equilibrate node is activated, the inverted bit line is shorted to the biasing node, thus biasing the inverted bit line; *(see Fig 1-2 of the prior art)*; the improvement comprising: elimination of one the second third transistors, allowing the biasing node to be located next to remaining of the second and third transistor, without widening circuit area. *See. Figs. 1-3; Cols. 3-5.*

Maki discloses the claimed invention as note above but not explicitly discloses wherein the memory device is a dynamic random access memory device. However, Maki disclose that

the present invention can apply to not only a SRAM circuit, but also various kinds of memory circuits in which signal line pair are precharged. It would have been obvious to one having ordinary skill in the art at the time of the invention to modify by form a dynamic random access memory (DRAM) of Maki's memory that connected to the precharge circuit to provide size reduction, high-speed, efficiency precharge circuit. *See Cols. 5-6.*

Regarding to claims 4-5, 8-9, 11-12, 14-15 as understood by examiner, Maki further discloses wherein the biasing node is connected to a current-liming device (VDD), but lack an inclusion of wherein an n-channel substrate contact can be located next to the current limiting device/biasing note without widening circuit area. However, Maki's PMOS transistors of the precharge circuit would inherently include n-channel substrate contact and that can be located next to the current limiting device/biasing noted without widening circuit area. If not, it would having obvious to one having ordinary skill in the art at the time of the invention to form an n-channel substrate contact of Maki's memory that can be located next to the current limiting device/biasing noted without widening circuit area to provide size reduction, high-speed, efficiency precharge circuit. *Note. Figs 1-3, Cols. 2-3 of Koike et al. cited to support well known position.*

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Lam whose telephone number is 571-272-1782. The examiner can normally be reached on 6:00 – 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoai Ho can be reached on 571-272-1777. The fax phone numbers for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

D. Lam

March 21, 2005

DAVID LAM
PRIMARY EXAMINER